

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Hiroki SHINKAWATA

Serial No.: 09/766,846

Filed: January 23, 2001

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME

THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	15	20	0	\$18.00 =	\$0.00
Independent Claims	1	3	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
					\$0.00
Total of Above Calculations					\$0.00

Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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Docket No.: 50090-275

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Hiroki SHINKAWATA :

Application No.: 09/766,846 :

Group Art Unit: 2811

Filed: January 23, 2001 :

Examiner: H. Vu

For: SEMICONDUCTOR DEVICE WITH TRANSFER GATE HAVING GATE
INSULATING FILM AND GATE ELECTRODE LAYER (AS AMENDED)

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AMENDMENT

Box Non-Fee Amendment

The Commissioner for Patents and Trademarks
Washington, DC 20231

Sir:

The following Amendment and Remarks are submitted in response to the Office Action
dated February 14, 2002. Please amend the above-identified application as follows:

IN THE TITLE:

Please replace "SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING
SAME" with --SEMICONDUCTOR DEVICE WITH TRANSFER GATE HAVING GATE
INSULATING FILM AND GATE ELECTRODE LAYER--.

Subt B²
IN THE CLAIMS:

A1

2. (Amended) The semiconductor device according to claim 1, further including a memory
cell section having a plurality of memory cells,